

New BERTScope™ Stressed Pattern Generator **Calibrated Stressed Data Generation at Flexible Bit Rates**

August 28, 2006 – MENLO PARK, California – SyntheSys Research, a developer and manufacturer of high-speed signal integrity test and measurement solutions for the computer, storage, and communications industries, introduces the new BERTScope S Pattern Generator.

The new BERTScope S Pattern Generator allows design and test engineers to generate calibrated, stressed data for jitter tolerance testing when either the device under test or a legacy BERT are used to measure bit error ratio. With very flexible clocking capabilities from 0.1 to 12.5 Gb/s, it can also stress an external clock, including spread spectrum clocks (SSC) for serial bus testing.

“Our customers have been asking for a flexible product that addresses their stressed data requirements at a reasonable cost,” said Lutz Henckels, President and CEO of SyntheSys Research. “We are pleased to be offering yet another first-to-market solution that responds to their needs.”

The BERTScope S Pattern Generator represents an entry point to the BERTScope product line, creating a cost-effective upgrade path to the flagship BERTScope S Analyzer.

Availability

Delivery of the BERTScope S Pattern Generator is 8 weeks ARO.

About BERTScope™

BERTScope™ is a trademark of SyntheSys Research, Inc., a privately held California corporation. Founded in 1989, its mission is to develop advanced test instruments for identifying and locating the source of errors in high-speed digital bit streams. BERTScope CR pairs with BERTScope to offer the vision of a scope, the confidence of a BERT, and clock recovery you can count on. More information is available at www.bertscope.com.

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