

First complete PLL analyzer tests PCIe compliance

MENLO PARK, CA – August 4, 2007 – SyntheSys Research, Inc., introduces the new BERTScope PLA series of Phase Locked Loop Analyzers – the first single instrument solution for validating that the response of PLLs (used for transmitting clock generation in Add-In cards) is compliant to PCI-Express test specifications.

Conventional approaches use multiple instruments and require complicated setup, cabling, and calibration. The BERTScope PLA simply requires the user to connect the four included cables to the PCI-SIG specified Compliance Base Board test fixture and connect the included USB cable to a PC. Once the control and display software is loaded from the included CD-ROM, the user is ready to test.

Verification of the PLL loop bandwidth and maximum peaking is a mandated test for validating compliance of PCIe Add-In cards operating at 5 GT/s data rates (generation 2) and a recommended test for validating the compliance of 2.5 GT/s generation 1 cards. Verifying the loop response parameter requirements are met is necessary to assure total system jitter is within budget, a critical factor at this high data rate. Traditional testing methods based on a spectrum analyzer and signal generator are cumbersome to set up, lack measurement resolution and repeatability, and require longer test times.

The new instruments improve measurement confidence and repeatability by obtaining high accuracy with amplitude resolutions up to 100 times greater than spectrum analyzers. The test is fast – less than 15 seconds for a complete response scan – providing the throughput to allow characterizing a larger number of samples for improved statistical confidence.

The BERTScope PLA instruments provide additional data, including phase response, which is useful to the engineer characterizing their PLL design.

The BERTScope PLA is available in two models. The base model PLL-PCIE is dedicated to PLL response compliance verification. The CRJ 12500A-PCIE is based on the BERTScope CRJ, the highest performance instrumentation-grade adjustable clock recovery product available today. In addition to PLL response compliance verification, this product provides all of the clock recovery, jitter spectral analysis, and Duty Cycle Distortion measurements available in the BERTScope CRJ 12500A.

About SyntheSys Research, Inc.

Founded in 1989, SyntheSys Research, Inc., innovator of the award-winning BERTScope™, is a privately held corporation located in Menlo Park, California. SyntheSys develops and manufactures high-speed signal integrity test and measurement instrumentation for the computer, storage and communications industries. Learn more at www.bertscope.com.

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