

## **First BER-Based Jitter Decomposition Including Jitter Separation on PRBS-31 and PRBS-23 for Compliance to 8 GT/s PCI Express 3.0 and DisplayPort 5.4 Gb/s**

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MENLO PARK, CA, February 2nd, 2009 – SyntheSys Research, Inc., introduces the new BERTScope Jitter Map Software Option. Jitter Map separates Total Jitter (TJ) into its sub-components, providing insight into jitter problems for design engineers, and making compliance testing easy with automated measurements for standards such as Fibre Channel, SFP+ (SFF-8431), IEEE 802.3aq (10GBASE-LRM), DisplayPort, PCI Express (PCIe) 2.0 and 3.0 (in draft), and IEEE 802.3ap (10GBASE-KR).

A major breakthrough enabled by Jitter Map is the ability to decompose jitter on patterns longer than PRBS-15, such as PRBS-23 and PRBS-31. These have long been used in testing high-speed digital optical communications devices and interfaces in applications such as 10 Gigabit Ethernet (10GbE, IEEE 802.3ae-2002), OIF-CEI 2.0, SFP+, XFP, and 40 and 100 GbE (IEEE 802.3ba, draft). Long patterns are also starting to appear in standards in draft form such as PRBS-23 in 8 GT/s PCIe 3.0 and PRBS-16 in DisplayPort 5.4 Gb/s. Engineers can run Jitter Map directly on patterns up to length PRBS-15, or use Long Pattern Jitter Triangulation Mode to perform jitter separation on longer data patterns as well as live packetized data, provided that Jitter Map can first be run using a shorter synchronized data pattern.

BER-based jitter measurement has long been the gold standard in measuring TJ, and for the first time is used to perform jitter separation of TJ into Random Jitter (RJ) and the many contributing components of Deterministic Jitter (DJ). Additional automated measurements make for easy compliance testing. For example, Sub-rate Jitter (SRJ), allows engineers to quantify many user-defined sub-rates including F/2 Jitter (a.k.a. F2 Jitter), which is jitter on every other bit regardless of its logic value and is used in standards such as 10GBASE-KR and the draft form of 8GT/s PCIe 3.0.

Visit the BERTScope Booth 619 at DesignCon 2009 in Santa Clara, CA, to see a live demo of Jitter Map.

### **Availability**

The BERTScope Option JMAP is available 12 weeks ARO.

### **About SyntheSys Research, Inc.**

SyntheSys Research, Inc., innovator of the award-winning BERTScope™, is a privately held corporation located in Menlo Park, California. SyntheSys develops and manufactures high-speed signal integrity test and measurement instrumentation for the computer, storage and communications industries. Learn more at [www.bertscope.com](http://www.bertscope.com).

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